Product Specification

400G OSFP to 2x 200G QSFP56 Active Optical Breakout Cable

PN:O400-2Q200-A

Features

- Hot Pluggable OSFP and QSFP56 form factor
- Available length range 1~50m
- Active Optical Cable
- 400Gb/s to 2x200Gb/s data rate
- Single +3.3V power supply
- Max power dissipation 400G≤8W, 200G≤4W
- 4-channel full-duplex active optical cable from
- Commercial temperature range 0°C to 70°C

Compliance

- Compliant with OSFP MSA and QSFP56 MSA
- Compliant with QSFP Electrical MSA SFF-8636
- Compliant with QSFP Mechanical MSA SFF-8665
- Compliant with CMIS 5.1
- IEEE 802.3bm
- RoHS

Applications

- 400G/200G Ethernet
- High Performance Computing (HPC)
- Data Center Interconnect
- Infiniband Devices

Description

The O400-2Q200-A is an Infiniband Active Optical Cable (AOC) designed to bridge 400G OSFP interfaces with legacy 200G QSFP56 infrastructure, enabling hybrid connectivity between next-gen switches and existing HDR/HCA devices. It splits a single 400Gb/s OSFP port into two independent 200Gb/s QSFP56 channels using eight multimode fiber pairs, distributing bandwidth via SFF-8665-compliant connectors. Built-in EEPROMs on both ends provide real-time diagnostics for temperature, signal quality, and firmware status, compatible with Infiniband management protocols. Rigorous production testing ensures error-free operation across industrial temperature ranges.

This splitter cable simplifies hybrid network architectures by eliminating intermediate adapters – for example, connecting a modern 400G OSFP switch directly to two 200G QSFP56 servers or storage nodes. Its active optical design reduces power consumption by 30% compared to copper alternatives while maintaining ultra-low latency (<5ns inter-channel skew), critical for synchronized AI/ML training clusters and high-frequency trading systems. The flexible, low-profile cabling supports dense rack deployments without airflow obstruction.

Ideal for phased Infiniband upgrades, it preserves investments in HDR-era hardware while unlocking NDR-ready switch capabilities. Hot-swappable functionality and backward compatibility allow seamless integration into 24/7 operational environments, minimizing downtime during maintenance. The solution optimizes total cost of ownership through reduced cabling complexity, energy efficiency, and extended compatibility with both current and emerging Infiniband standards.

Product performance Specifications

1、Basic Product Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	3.135	3.3	3.465	V
Supply noise tolerance (10Hz – 10MHz)	V_{CC}	66	-	-	mVpp
Relative Humidity	RH	5	-	85	%
Operating Case Temperature	T_C	0	-	70	°C
Power consumption 200Gb/s end	PWR	-	3.5	4	W
Power consumption 400Gb/s end	PWR	-	7.5	8	W

2、OSFP Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Transmitter					
AC Common-mode Output Voltage(RMS)				17.5	mV
Differential Peak-to-peak Output Voltage(Transmitter disabled)				35	mV
Differential Peak-to-peak Output Voltage(Transmitter enabled)				880	mV
Eye Symmetry Mask Width	ESMW		0.22		UI
Eye Height, Differential	EH	32			mV
Differential Output Return Loss		See Note1			
Common to differential mode conversion return loss		See Note2			
Differential termination mismatch		10			%
Transition time (20% to 80%)	Tr,Tf	10			ps
Receiver					
Far-end Eyeheight, differential		30			mV
Far-endpre-cursor ISI Ratio		-4.5		2.5	%
Differential Output Return Loss		See Note1			
Common to Differential Mode Conversion Return Loss			See Note2		
Differential Termination Mismatch		10			%
Transition Time (20% to 80%)	Tr,Tf	10			ps
DC Common Mode Voltage		-350		2850	mV

Note1: $\mathrm{RLd(f)} \geq \{^{9.5-0.37\mathrm{f}}_{4.75-7.4\log_{10}(\frac{\mathrm{f}}{14})}{}^{0.01\leq \mathrm{f}<8}_{8\leq \mathrm{f}<19}\}(\mathrm{dB})$ where f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss.

Note2: $\mathrm{RLdc(f)} \geq \{^{22-20(\frac{\mathrm{f}}{25.78})}_{15-6(\frac{\mathrm{f}}{25.78})}{}^{0.01\leq \mathrm{f}<12.89}_{12.89\leq \mathrm{f}<19}\}(\mathrm{dB})$ where f is the frequency in GHz, RLdc is the CAUI-4 Chip-to-module input differential return loss.

3、QSFP Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Transmitter					
AC Common-mode Output Voltage(RMS)				17.5	mV
Differential Peak-to-peak Output Voltage(Transmitterdisabled)				35	mV
Differential Peak-to-peak Output Voltage(Transmitterenabled)				880	mV
Eye Symmetry Mask Width	ESMW		0.22		UI
Eye Height, Differential	EH	32			mV
Differential Output Return Loss		See Note1			
Common to differential mode conversion return loss		See Note2			
Differential termination mismatch		10			%
Transition time (20% to 80%)	Tr,Tf	10			ps
Receiver					
Far-end Eyeheight, differential		30			mV
Far-endpre-cursor ISI Ratio		-4.5		2.5	%
Differential Output Return Loss		See Note1			
Common to Differential Mode Conversion Return Loss		See Note2			
Differential Termination Mismatch		10			%
Transition Time (20% to 80%)	Tr,Tf	10			ps
DC Common Mode Voltage		-350		2850	

Note1: $\mathrm{RLd(f)} \geq \begin{cases} 9.5 - 0.37\mathrm{f} & 0.01 \leq \mathrm{f} < 8 \\ 4.75 - 7.4\log_{10}(\frac{\mathrm{f}}{14}) & 8 \leq \mathrm{f} < 19 \end{cases} (\mathrm{dB})$ where f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss.

Note2: $\mathrm{RLdc(f)} \geq \begin{cases} 22 - 20(\frac{\mathrm{f}}{25.78}) & 0.01 \leq \mathrm{f} < 12.89 \\ 15 - 6(\frac{\mathrm{f}}{25.78}) & 12.89 \leq \mathrm{f} < 19 \end{cases} (\mathrm{dB})$ where f is the frequency in GHz, RLdc is the CAUI-4 Chip-to-module input differential return loss.

Recommended Host Board Power Supply Circuit

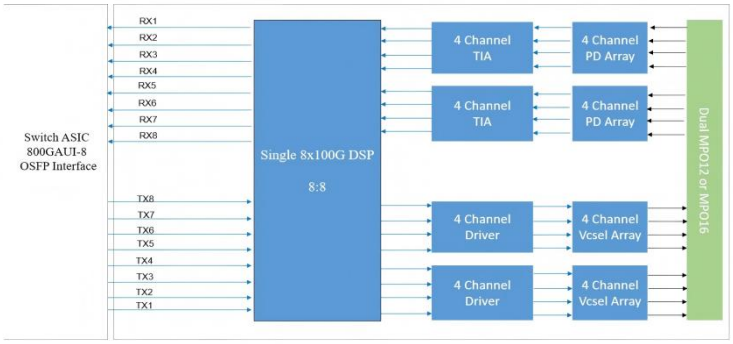


Figure 1: Module Block Diagram

Recommended Interface Circuit

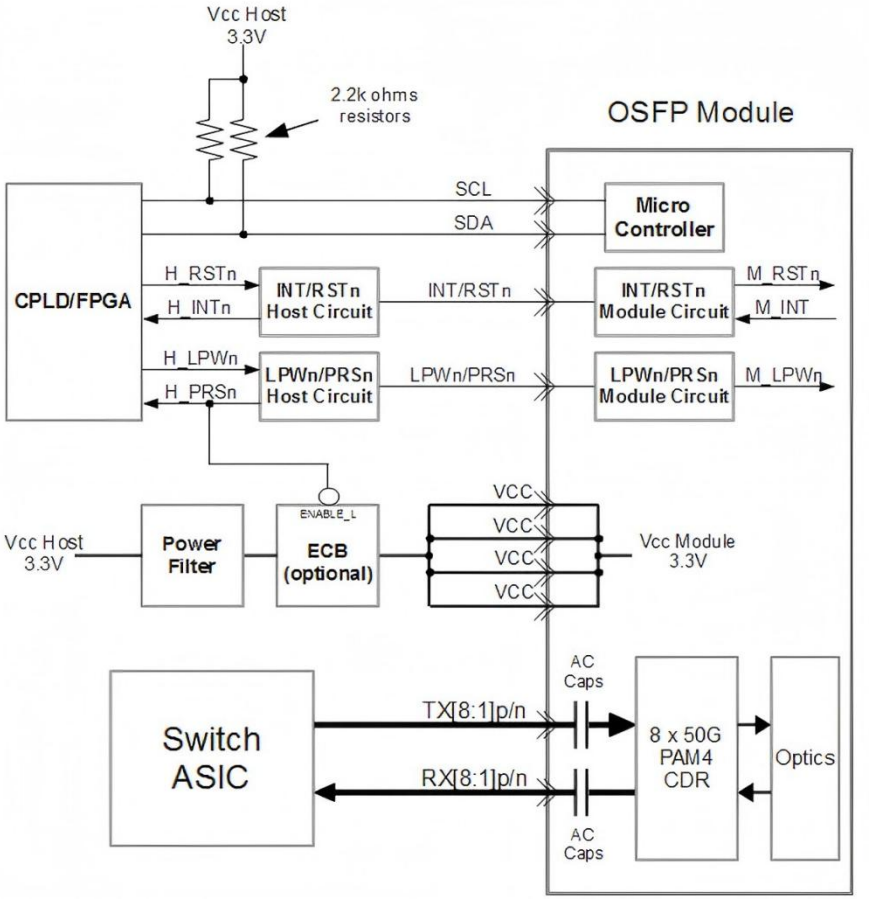


Figure2: Recommended Interface Circuit

OSFP Pin-out Definition

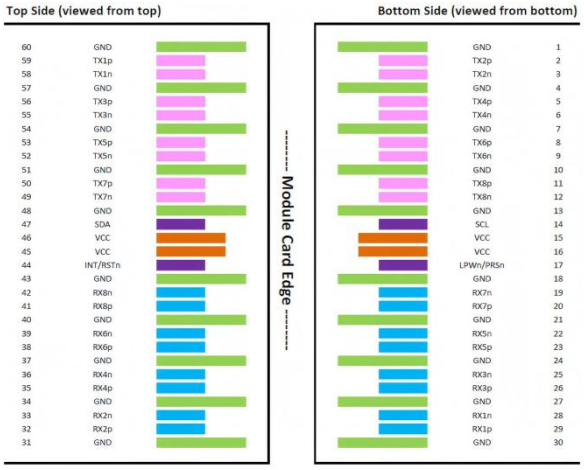


Figure3:OSFP Pin view

OSFP Pin Function Definitions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	1
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	2
18		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	

21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	2
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	1
48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	
50	CML-I	TX7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	

59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Note1: Open-Drain with pull up resistor on Host.

Note2: See pin description for required circuit.

QSFP Pin-out Definition

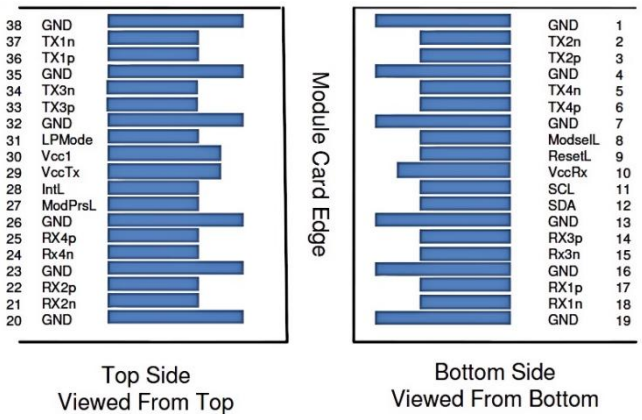


Figure4:QSFP Pin view

QSFP Pin Function Definitions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	4
9	LVTTL-I	ReSelL	Module Select	4
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	4
12	LVCMOS-I/O	SDA	2-wire serial interface data	4
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3
19		GND	Ground	1

20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output Ground	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	4
28	LVTTL-O	IntL	Interrupt	4
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	4
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3
38		GND	Ground	1

Note1:GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Note3: High-speed signal interfaces require differential pairs (e.g. TX1+/TX1-) with tightly matched impedances (typically 100Ω).

Note4: The management and control signals are based on LVTTL level logic and are used for functions such as module selection and reset.

OSFP Monitoring Specification

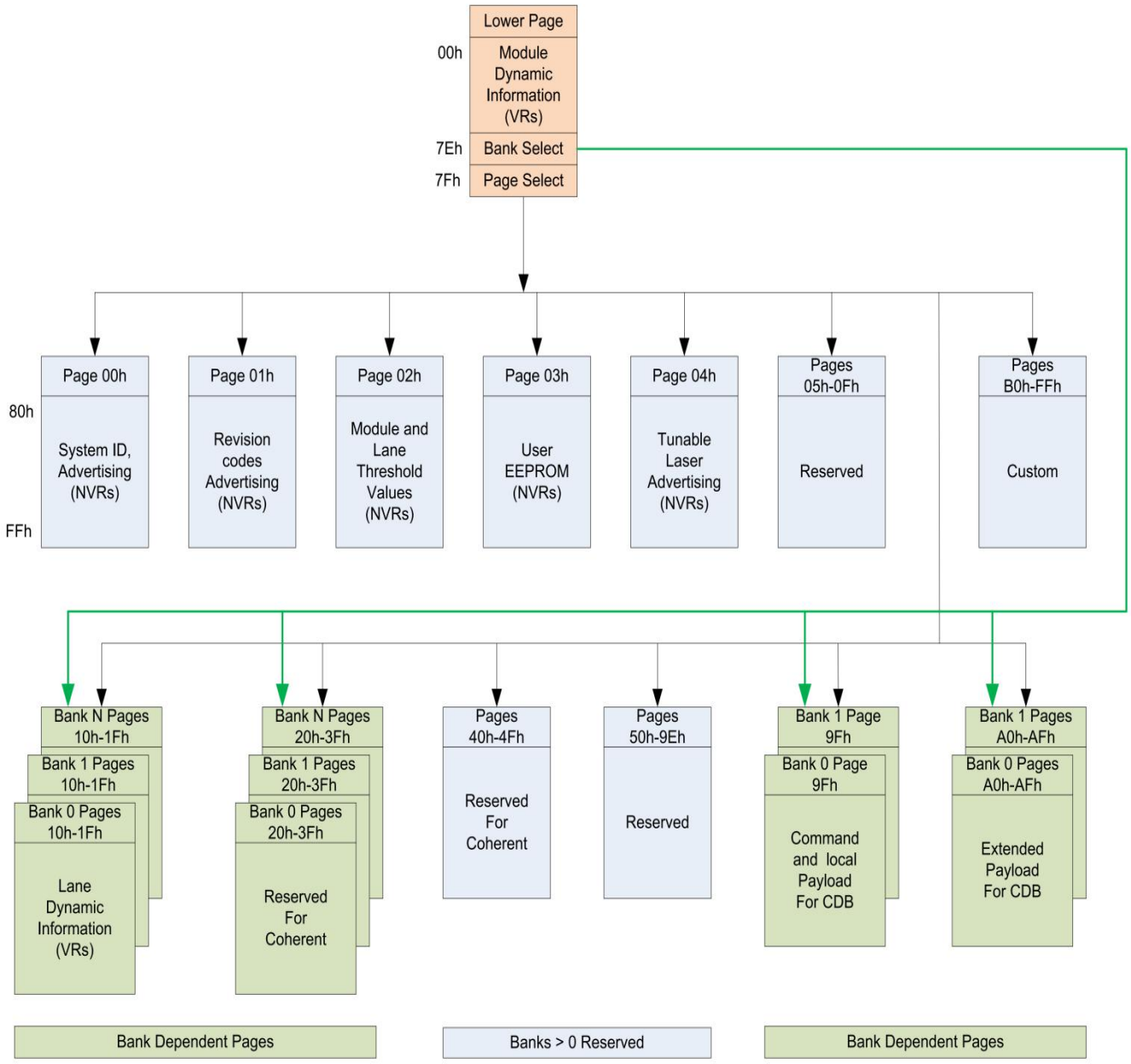


Figure5: Memory map

OSFP Memory map Table

Byte	Unit	Name	Description
		Lower Page 00h	
0	1	Identifier	Identifier - Type of Serial Module - See SFF-8024.
1	1	Revision Compliance	Identifier – CMIS revision; the upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.
2-3	2	ID and Status Area	Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal.
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh.
8-13	6	Module-Level Flags	All flags that are not lane or data path specific.
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific.
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	Password Entry and Change
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page
		Upper Page 00h	
128	1	Identifier	Identifier - Type of Serial Module - See SFF-8024.
129-144	16	Vendor name	Vendor name (ASCII)
145-147	2	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	8	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	10	Vendor SN	Vendor Serial Number (ASCII)
182-183	2	Date code year	ASCII code, two low order digits of year (00=2000)
184-185	2	Date code month	ASCII code digits of month (01=Jan through 12=Dec)
186-187	2	Date code day of month	ASCII code day of month (01-31)
188-189	2	Lot code	ASCII code, custom lot code, may be blank
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	Module power characteristics

202	1	Cable assembly length	Cable assembly length
203	1	Media Connector Type	Media Connector Type
204	1	5 GHz attenuation	Passive copper cable attenuation at 5 GHz in 1 dB increments
205	1	7 GHz attenuation	Passive copper cable attenuation at 7 GHz in 1 dB increments
206	1	12.9 GHz attenuation	Passive copper cable attenuation at 12.9 GHz in 1 dB increments
207	1	25.8 GHz attenuation	Passive copper cable attenuation at 25.8 GHz in 1 dB increments
208-209	2	Reserved	Reserved
210-211	2	Cable Assembly Lane Information	Cable Assembly Lane Information
212	1	Media Interface Technology	Media Interface Technology
213-220	8	Reserved	Reserved
221	1	Custom	Custom
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	Custom Info NV

QSFP Monitoring Specification

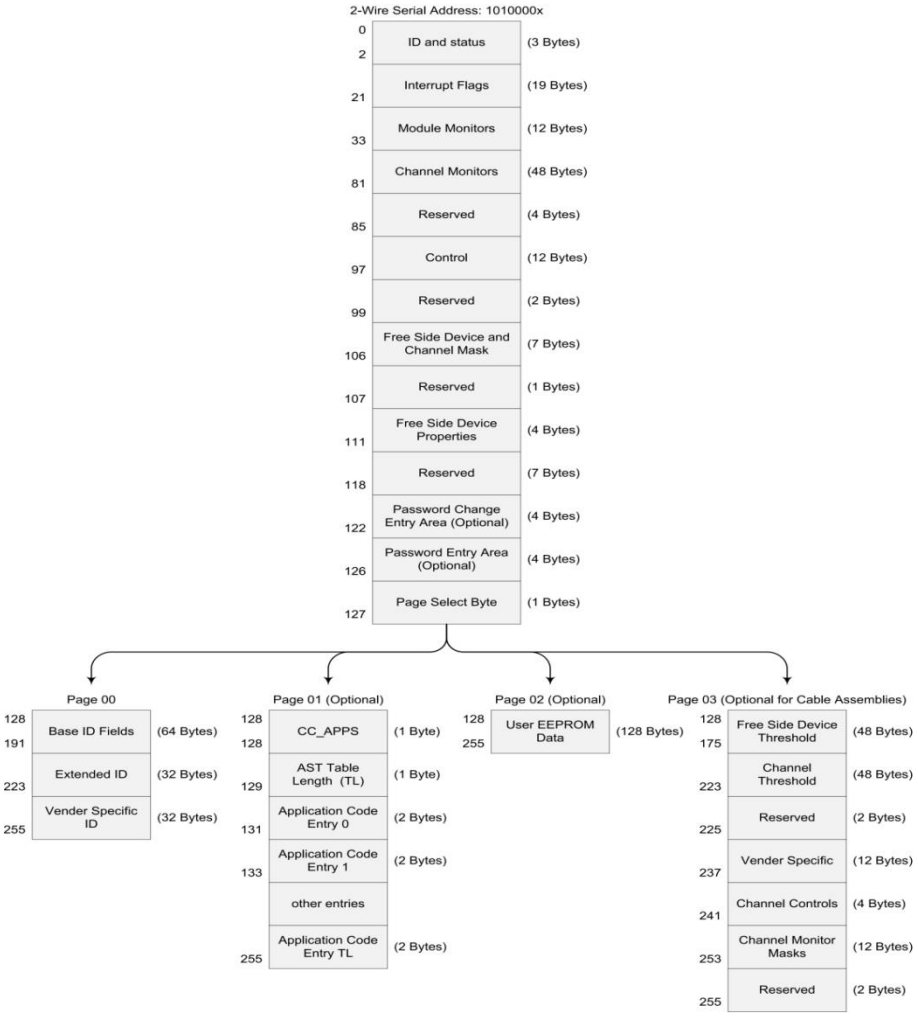


Figure6:QSFP Memory map

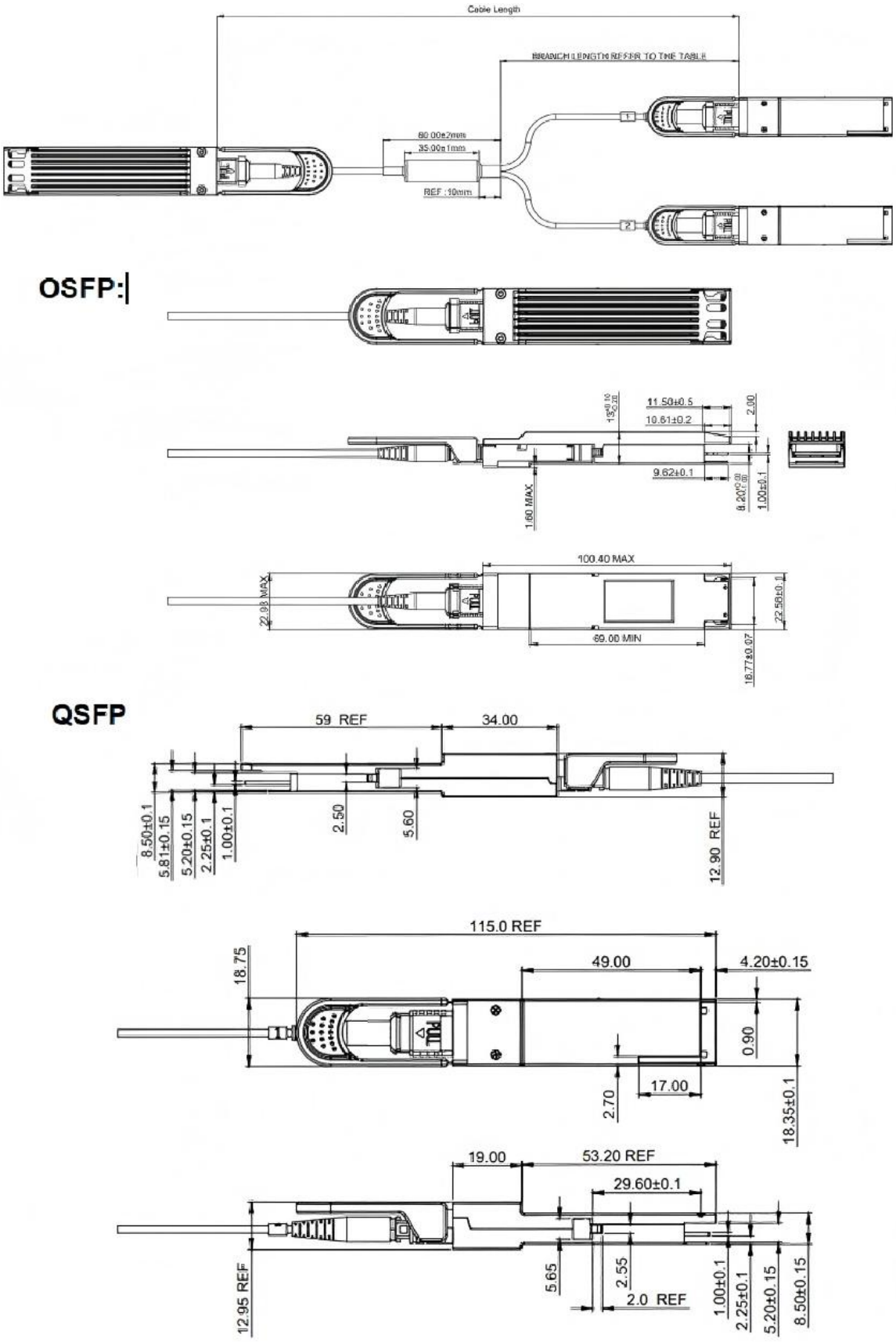
QSFP Memory map Table

Byte	Unit	Name	Description
		Lower Page 00h	
0	1	Identifier	Type of transceiver,Page 00h Byte 0 and Page 00h Byte 128 shall contain the same parameter values.
1	1	Status	Revision Compliance
2	1	Status	Status indicators
3-21	19	Interrupt Flags	Consist of interrupt flags for LOS, Tx Fault, warnings and alarms. The non-asserted state shall be 0b.
22	1	Temperature MSB	Internally measured temperature (MSB)
23	1	Temperature LSB	Internally measured temperature (LSB)
24-25	2	Reserved	Reserved
26	1	Supply Voltage MSB	Internally measured supply voltage (MSB)
27	1	Supply Voltage LSB	Internally measured supply voltage (LSB)
28-29	2	Reserved	Reserved
30-33	4	Vendor Specific	Vendor Specific
34	1	Rx1 Power MSB	Internally measured Rx1 input power
35	1	Rx1 Power LSB	
36	1	Rx2 Power MSB	Internally measured Rx2 input power
37	1	Rx2 Power LSB	
38	1	Rx3 Power MSB	Internally measured Rx3 input power
39	1	Rx3 Power LSB	
40	1	Rx4 Power MSB	Internally measured Rx4 input power
41	1	Rx4 Power LSB	
42	1	Tx1 Bias MSB	Internally measured Tx1 bias
43	1	Tx1 Bias LSB	
44	1	Tx2 Bias MSB	Internally measured Tx2 bias
45	1	Tx2 Bias LSB	
46	1	Tx3 Bias MSB	Internally measured Tx3 bias
47	1	Tx3 Bias LSB	
48	1	Tx4 Bias MSB	Internally measured Tx4 bias
49	1	Tx4 Bias LSB	
50	1	Tx1 Power MSB	Internally measured Tx1 Power
51	1	Tx1 Power LSB	
52	1	Tx2 Power MSB	Internally measured Tx2 Power
53	1	Tx2 Power LSB	
54	1	Tx3 Power MSB	Internally measured Tx3 Power
55	1	Tx3 Power LSB	
56	1	Tx4 Power MSB	Internally measured Tx4 Power

57	1	Tx4 Power LSB	
58-65	8	Reserved	Reserved channel monitor set 4
66-73	8	Reserved	Reserved channel monitor set 5
74-81	8	Vendor Specific	Vendor Specific
82-85	4	Reserved	Reserved
86-99	14	Control	Control
100-106	7	Free Side Device and Channel Masks	Free Side Device and Channel Masks
107-110	4	Free Side Device Properties	Free Side Device Properties
111-112	2	Assigned for use by PCI Express	Used for: - The PCI Express External Cable Specification - The PCI Express OCuLink Specification
113-117	4	Free Side Device Properties	Free Side Device Properties
118	1	Reserved	Reserved
119-122	4	Password Change Entry Area	Password Change Entry Area
123-126	4	Password Entry Area	Password Entry Area
127	1	Page Select Byte	Page Select Byte
Upper Page 00h			
128	1	Identifier	Identifier Type of free side device.(See SFF-8024 Transceiver Management)
129	1	Ext. Identifier	Extended Identifier of free side device. Includes power classes, CLEI codes, CDR capability.
130	1	Connector Type	Code for media connector type. (See SFF-8024 Transceiver Management)
131-138	8	Specification Compliance	Code for electronic or optical compatibility.
139	1	Encoding	Code for serial encoding algorithm. (See SFF-8024 Transceiver Management)
140	1	Signaling rate, nominal	Nominal signaling rate, units of 100 MBd. For rate > 25.4 GBd, set this to FFh and use Byte 222.
141	1	Extended Rate Select Compliance	Tags for extended rate select compliance.
142	1	Length (SMF)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for SMF fiber in km *. A value of 1 shall be used for reaches from 0 to 1 km.
143	1	Length (OM3 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for EBW 50/125 um fiber (OM3), units of 2 m *
144	1	Length (OM2 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 50/125 um fiber (OM2), units of 1 m *

145	1	Length (OM1 62.5 um) or Copper Cable Attenuation	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 62.5/125 um fiber (OM1), units of 1 m *, or copper cable attenuation in dB at 25.78 GHz.
146	1	Length (passive copper or active cable or OM4 50 um)	Length of passive or active cable assembly (units of 1 m) or link length supported at the signaling rate in byte 140 or page 00h byte 222, for OM4 50/125 um fiber (units of 2 m) as indicated by Byte 147. See 6.3.12.
147	1	Device technology	Device technology
148-163	16	Vendor name	Free side device vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand.
165-167	3	Vendor OUI	Free side device vendor IEEE company ID.
168-183	16	Vendor PN	Part number provided by free side device vendor(ASCII)
184-185	2	Vendor rev	Revision level for part number provided by the vendor(ASCII)
186-187	2	Wavelength or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5 GHz (Byte 186) and 5.0 GHz (Byte 187)
188-189	2	Wavelength tolerance or Copper Cable Attenuation	The range of laser wavelength (+/- value) from nominal wavelength. (wavelength Tol. =value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12.9 GHz (Byte 189)
190	1	Max case temp	Maximum case temperature
191	1	CC_BASE	Check code for base ID fields (Bytes 128-190)
192	1	Link codes	Extended Specification Compliance Codes (See SFF-8024)
193-195	3	Options	Optional features implemented.
196-211	16	Vendor SN	Serial number provided by vendor.(ASCII)
212-219	8	Date Code	Vendor's manufacturing date code.
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the free side device. Bit 1,0 Reserved.
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the free side device.
222	1	CC_EXT	Check code for the Extended ID Fields (Bytes 192-222)
224-255	32	Vendor Specific	Vendor Specific EEPROM

Mechanical Dimension



Note:

- Diameter: 3mm
- Minimum bend radius:30mm
- Cable color:Orange(OM2),Aqua(OM3),Magenta(OM4)
- When L≤1m, the tolerance is +5cm
- When 1m≤L≤4.5m, the tolerance is +15cm
- When 5m≤L≤14.5m, the tolerance is +30cm
- When L≥15m, the tolerance is +2%m

Waring:

- The transceiver optics is supplied with a dust cover. This plug protects the transceiver optics during standard manufacturing processes by preventing contamination from air borne particles.It is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.
- Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.
- Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.